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REMARKS

By this amendment, claims 8-12 are canceled, claim 7 has been amended, and claims 14-20 are new. No new matter has been entered. Accordingly, claims 1-7, and 13-20 are pending in this application.

In the Office Action, Han et al is cited against the recited invention but neither was the reference provided nor a patent number listed on the Examiner's Reference Sheet. Applicants have assumed that this was a typographical error, and instead meant to cite Rodder. Otherwise, the Examiner is requested to forward the reference such that it may be considered in another non-final office action.

The Examiner has objected to claims 7 and 8 on the basis of presentation and form. Claims 9-12 are objected to on the basis of lack of indefiniteness. Such objections have been overcome by the above amendments.

In the Office Action, the examiner rejected claims 1-4 under 35 USC 103(a) as being unpatentable over Takahashi et al (US 6,657,893) in view of Wu (US 6,649,308) and Colabella (US 6,252,274). The examiner rejected claim 5 as being unpatentable over Takahashi et al in view of Wu and Colabella, as applied to claims 1-4 and further in view of Sung et al (US 6,417,049). The examiner rejected claim 6 as being unpatentable over Colabella in view of Wu and Rodder (US 6,239,225). The examiner rejected claims 7 and 8 as being unpatentable over Colabella in view of Wu and Rodder, as applied to claim 6, and further in view of Liu et al (US 5,094,984) and Sobek et al (US 6,268,624). The examiner rejected claims 9-12 as being unpatentable over Colabella in view of Wu, and claim 13 as being unpatentable over Madurawe et al (US 6,646,919) in view of Colabella, Wu and [Rodder?].

In rejecting the claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. See *In re Rijckaert*, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). A prima facie case of obviousness is established by presenting evidence that would have led one of ordinary skill in the art to combine the relevant teachings of the references to arrive at the claimed invention. See *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988) and *In re Lintner*, 458 F.2d 1013, 1016, 173 USPQ 560, 562 (CCPA 1972).

In reviewing the office action, the examiner has combined the teachings of a number of references in order to reach a conclusion of obviousness. When an obviousness determination is based on multiple prior art references, there must be a showing of some "teaching, suggestion, or reason" to combine the references. Evidence of a suggestion, teaching, or motivation to combine prior art references may flow, inter alia, from the references themselves, the knowledge of one of ordinary skill in the art, or from the nature of the problem to be solved. Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form, must nevertheless be "clear and particular." *Winner International Royalty Corp. v. Wang*, 202 F.3d 1340, 53 USPQ2d 1580 (Fed. Cir. 2000).

Applicants are aware that most if not all inventions arise from a combination of old elements. See *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457 (Fed. Cir. 1998). Thus, every element of a claimed invention may often be found in the prior art. See id. However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. See id. Lastly, in determining obviousness/nonobviousness, an invention must be considered "as a whole," 35 U.S.C. § 103, and claims must be considered in their entirety. *Medtronic, Inc. v. Cardiac Pacemakers, Inc.*, 721 F.2d 1563, 1567, 220 USPQ 97, 101 (Fed. Cir. 1983).

In the rejection, the examiner asserts that it would have been obvious at the time the invention was made to a person of ordinary skill in the art to take the semiconductor device of Takahashi et al (US 6,657,893) and modify it by using the self-aligned source of Colabella (US 6,252,274) and the phosphorous-doped side wall spacers of Wu (6,649,893) in order to produce the recited invention of claims 1-4. The examiner also rejected claim 5 as being unpatentable over Takahashi et al in view of Wu and Colabella, as applied to claims 1-4 and further in view of Sung et al (US 6,417,049) for teaching worlines formed from the second polysilicon. The applicants respectfully traverse these rejections for the following reasons.

In our view, it would not have been obvious at the time the invention was made to a person of ordinary skill in the art to have modified Takahashi et al in view of Colabella and Wu to arrive at the claimed subject matter. In that regard, the invention when considered "as a whole" as required by 35 U.S.C. § 103 is not suggested by the applied prior art.

First, Takahashi et al teach providing in each of their memory cell an additionally transistor (the select Tr) coupled to a memory transistor (the Memory Tr) via an intermediate region 10, wherein the drain 8 is provided adjacent the memory transistor and the source is provided adjacent the select transistor. See FIG. 1, and column 21, line 31-36. As shown the intermediate region 10 separates gate insulating films 4 and 11. Accordingly, in addition to failing to disclose the use of self-aligned source (SAS) regions and the presence of a phosphorous-doped oxide along the vertical edges of the gate stack, Takahashi et al also fail to disclosure providing "a first oxide layer deposited over the substrate stretching from the drain to the self-aligned source," as recited by claim 1. Extending the first oxide layer from the drain to the self-aligned source, such as disclosed by Colabella, in order to produce this limitation of the claim 1 would completely render the device of Takahashi et al. useless for its intended purpose. None of the other cited references would cure this deficiency in the combination of references.

Second, Takahashi et al. are addressing problems associated with a FN-FN type flash EEPROM and not a CHE type flash EEPROM. One skilled in the art understands that the present invention is directed to a CHE-type flash EEPROM as the source 101 is deeper than the drain 102 as depicted in FIG. 1.

Third, one skilled in the art is not provided with the motivation to combine the teachings of Takahashi et al and Colabella. Colabella is directed to addressing the problem of the leakage current 15 flowing beneath the bit line between the source line 10 and the drain line 17 of a CHE type flash EEPROM, and not a FN-FN type flash EEPROM as in the case of Takahashi et al. See Fig. 2B and note that the source region is deeper than the drain region. To address the above problem, Colabella teaches the steps of providing a 585 mask for the P ands As source implantation, removing the 585 mask, and then performing later an As source and drain implantation. See col. 5, lines 33-39. Accordingly, the source and drain of Colabella after the SAS process are not symmetrical. Takahashi et al stipulate that regions 8, 9, and 10 are doped at the same time such that they have an equal dopant concentration, and therefore are formed symmetrically. See col. 21, lines 56-61. Accordingly, one skilled in the art reading Takahashi et al as a whole would not employ the SAS procedure of Colabella (col. 5, lines 22-44), as alleged by the examiner, as the two teach away from each other.

Finally, even if one skilled in the art did make the suggested combination, using the SAS process of Colabelle to produce a drain region deeper than a source region would most likely make the FN-FN type flash EEPROM of Takahashi et al. (even though specifically teaching to have equal doping concentrations and symmetrical source and drain regions), inoperable for its intended purpose. Such a resulting device having a source region deeper than a drain region is counter to prior art FN-FN type flash EEPROM designs, which operate by having equal or deeper drains than sources.

Applicants also note that there is no motivation to provide the phosphorous-doped oxide spacer of Wu to Takahashi et al. as suggested by the examiner. Wu provides the spacers to serve as a diffusion source to form the extended source and drain junction 24 for the minimum junction depth requirement. See col. 3, lines 7-11. Wu neither discloses nor suggests that forming such extended source and drain junctions with such a diffusion source for providing a minimum junction depth would benefit a FN-FN type EEPROM or even address any of the problems facing Takahashi et al. Takahashi et al. is silent on addressing problems of electrode sheet resistance and source/drain resistance, or the desire to provide extended source and drain junctions for a minimum junction depth.

As mentioned previously, Takahashi et al. explicitly teach that diffusion layers 8, 9, and 10 have an equal dopant concentration and the same depth, and therefore are formed symmetrically. Accordingly, as the source and drains regions 8 and 9 of Takahashi et al are separated by immediate region 10, it is unknown what effect extending such source drain regions under their respective transistor as taught by Wu would have on the device of Takahashi et al. None of the cited references purport that such a modification would be successful.

With regards to claim 5, modifying the device of Takahaski et al. in view of Sung et al (US 6,417,049), that is forming the wordline from the second polysilicon, clearly would make the device of Takahaski et al inoperable for its intended purpose. There would be no control over the select transistor of Takahashi et al if the wordline was formed from the second polysilicon. See Fig. 4(a).

As should be apparent from a reading of the examiner's rejection and the above points showing that there is no "clear and particular" reason for their combinations, the only possible suggestion for modifying the dual transistor device of Takahashi et al in the manner proposed by

the examiner to arrive at the recited subject matter of claims 1-5 in view of whole teachings of Colabella, Wu and Sung, is hindsight knowledge derived from the applicants' own disclosure. The examiner is reminded that in deciding the question of obviousness under 35 U.S.C. §103, it is not realistic to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such references fairly suggests to one of ordinary skill in the art. *In re Wesslau*, 353 F.2d 238, 241, 147 USPQ 391, 393 (CCPA 1965); see also *In re Mercer*, 515 F.2d 1161, 1165-66, 185 USPQ 774, 778 (CCPA 1975). The mere existence in the prior art of individual elements of applicants' invention does not, without more, render the claimed invention prima facie obvious under 35 U.S.C. §103. Instead, there must be evidence that the bringing together of such elements would have been prima facie obvious to a person of ordinary skill in the art. It follows that the examiner's rejections of claims 1-5 under 35 U.S.C. § 103 should be withdrawn.

Claim 6 is rejected as being unpatentable over Colabella in view of Wu and Rodder (US 6,239,225). In the rejection, the examiner determined that it would have been obvious at the time the invention was made to a person of ordinary skill in the art to take the semiconductor device of Colabella and modify it by using the phosphorous-doped side wall spacers of Wu and the re-oxidation profile of Rodder in order to produce the recited invention of claim 6. The applicants respectfully traverse this rejection for the following reasons.

As mentioned previously, Colabella is addressing the problem of the leakage current 15 flowing beneath the bit line between the source line 10 and the drain line 17. See Fig. 2B. Colabell asserts that their SASFOX process lowers the likelihood of current leaking into the bit line region (G) over the field oxide, by providing for an increased physical channel length (Lpar) while leaving the effective channel length (Leff) unchanged. See col. 6, lines 1-4. Colabella also provides a phosphorous dopant only to the source region. See col. 5, line 52-56. Wu on the other hand shortens the physical channel length (Lpar) by using the sidewall spacers to extend the source and drain region into shallow phosphorous doped regions under the spacers. Also Wu dopes both the source and drain regions with phosphorous. Clearly these references teach away from each.

As these references teach away from each other, it is unknown what effect substituting the isolation spacers 12 of Colabella with the phosphorous doped spacers of Wu. Doing so

would most likely change the diffusion profile in the source and drain regions, and could render the device of Colabella inoperable for its intended purpose. Rodder is cited for disclosing a re-oxidation profile, and therefore does not cure the above noted deficiencies and dissimilar teachings of Colabella and Wu. Again, the only possible suggestion for modifying the device of Colabella in the manner proposed by the examiner to arrive at the recited subject matter of claim 6 in view of Wu and Rodder, is hindsight knowledge derived from the applicants' own disclosure. It follows that the examiner's rejections of claim 6 under 35 U.S.C. § 103 should be withdrawn.

Claim 7 and 8 are rejected as being unpatentable over Colabella in view of Wu and Rodder, as applied to claim 6, and further in view of Liu et al (US 5,094,984) and Sobek et al (US 6,268,624). Claim 8 has been cancelled. Sobek et al is cited for teaching that the re-oxidation process results in inter layer encroachment and the development of a cuspate structure characterized by a "height" and a "width." Liu et al. is cited for teaching that PSG films are porous and highly hydroscopic, depending on the phosphorous concentration. Accordingly, none of these cited reference cure the above noted deficiencies in regards to unobvious claim 6 from which claim 7 depends. Additionally, none of the cited reference disclose or suggest that the width is a horizontal distance from a side edge of the first polysilicon layer to a vertical edge of the tunnel oxide layer, wherein the width is less than a re-oxidation oxide profile width without the phosphorous doped oxide layer as recited by amended claim 7. Please note, claim 7 was amended not for reasons of patentability in view of the prior art but to overcome the examiner's noted objection. Accordingly, withdrawal of the rejection to claim 7 is also requested.

Claims 9-12 are rejected as being unpatentable over Colabella in view of Wu. Claims 9-12 have been cancelled, of which the subject matter is represented as claims 14-18 in order to overcome the objections of the examiner and not for reasons of patentability in view of the prior art. As stated above, the only possible suggestion for modifying the device of Colabella in the manner proposed by the examiner to arrive at the recited subject matter of original claims 9-12 in view of Wu, in view of their opposed teachings is hindsight knowledge derived from the applicants' own disclosure. Therefore, it follows that claims 14-18 as presented are allowable over the cited art.

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Claim 13 is rejected as being unpatentable over Madurawe et al (US 6,646,919) in view of Colabella, Wu, and [Rodder?]. The applicants respectfully traverse this rejection for the following reasons. There is no FIG. 2A of Madurawe et al. which shows the features cited by the examiner. Applicants assume that the examiner meant FIGS. 1, 2A, and 3 of Colabella. Therefore, the examiner is asserting that one skilled in the art would substitute the memory device of Colabella for the flash memory device 1306 in FIG. 13 of Madurawe et al. However, the prior art memory device of Colabella can also be considered a double polysilicon process EEPROM which has a polysilicon control gate (line 13) capacitively coupled to its floating gate. See FIG. 2A. Madurawe et al. specifically teach that margin testing of single polysilicon process EEPROMs is the focus of their invention. See. col. 1, line 36-45. Madurawe et al. further state that "it should be apparent that in order to test a conventional EEPROM cell's erase margin (i.e., for the lower threshold voltage), the cell's control gate would have to be biased to a negative voltage. In a double poly cell this presents no problem since the control gate is isolated from other elements of the cell. However, in a single polysilicon process EEPROM, it is not possible to bias the control gate to a negative voltage." Understandably, Madurawe et al then continue to describe an apparatus and process to margin test a single poly EEPROM, and nowhere state the their invention can be used with a double poly cell. Accordingly, one skilled in the art is provided with no motivation to make such as substitution of a double poly cell of Colabella for a single poly cell of Madurawe as suggested by the examiner, as these reference teach away from each other. This inability to combine the cited reference is further acerbated by the opposed teachings of Colabella and Wu as noted previously above. Rodder fails to cure any of these problems with the asserted combination of references. Once again, the only possible suggestion for modifying the computer system of Madurawe et al. in the manner proposed by the examiner to arrive at claim 13 in view of Collabella, Wu, and [Rodder?] is hindsight knowledge derived from the applicants' own disclosure. Therefore, it follows that claim 13 as presented is also allowable over the cited art.

New claims 19 and 20 are directed to other embodiments not previously noted by the applicants, and for which protection is desired. Clearly, in view of all the arguments set forth above, claims 19 and 20 are also allowable over the cited art.

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The applicants believe that all claims are now in condition for allowance. The examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response.

Respectfully submitted,
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